REMARKS

This application has been carefully reviewed in light of the Final Office Action dated August 6, 2004. Claims 1-2, 5-8, 11-15, and 18-20 remain in this application. Claim 1 is the independent claim. Claim 1 has been amended. Claims 3-4, 9-10, 16-17, and 21 have been cancelled without prejudice. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Drawing Objections

The drawings were objected to under 37 CFR §1.83(a) for failing to show every feature of the invention specified in the claims. The Office Action purports that, "the display driver comprising a line data register, a column data register and an data generation circuit," as recited in Claim 4, is not shown in the drawings.

However, the originally filed drawings and specification show and disclose all the features of the claimed invention. Figure 9 of the present application shows a drive-system control circuit 170. Figure 8 of the present application shows a line data register 80, a column data register 82, and a data generation circuit 84 as recited in the claims.

Moreover, on page 13, lines 9-11, the present application discloses that the image determination data could also be generated by the X driver IC 28, or by the CPU 12 and the controller 14. On page 22, line 22-27, the present application discloses that the image determination data generation circuit includes a line data register 80, a column data register 82, and a data generation circuit 84. On page 28, line 12-14, the present application discloses the drive-system control circuit 170 includes the above described image determination data generation circuit.

Clearly, the originally filed drawings and specification show and disclose the features of the present invention as recited in the claims.

Claim Objections

Claim 4 was objected to under 37CFR §1.75(a) for indefiniteness. In response, Applicant has amended Claim 4 in accordance with the Examiner's suggestions. Applicant respectfully submits that Claim 4 is now in condition for allowance and such allowance is respectfully requested.

Non-Art-Based Rejections

Claims 4, 10, and 17 were rejected under 35 USC §112, first paragraph, for lack of antecedent support. According to the Office Action, the specification does not fairly teach the location of the image determination data generation circuit as part of the claimed invention.

However, the present application discloses an external image determination data generation circuit and an image determination data generation circuit. On page 5, line 21-23, the present application discloses, "Note that the image determination data could be generated within the display driver or it could be supplied from the exterior with other data". On page 6, line 15-18, the present application discloses, "the image determination data could be generated on the basis of column and line address within the display driver, or it could be image determination data that has been generated outside of the device".

Moreover, the present application discloses the location of the image determination data generation circuit within the claimed invention, which enables one skilled in the art to make and use the claimed invention. Figure 9 of the present application shows an embodiment of present invention to include a drive-system control circuit 170. Figure 8 of the present application shows a line data register 80, a column data register 82, and a data generation circuit 84 as recited in

the Claim 4. On page 13, lines 9-11, the present application discloses that the image determination data could also be generated by the X driver IC 28, or by the CPU 12 and the controller 14, by way of example. On page 22, line 22-27, the present application discloses that the image determination data generation circuit having a line data register 80, a column data register 82, and a data generation circuit 84. On page 28, line 12-14, the present application discloses that the drive-system control circuit 170 having the above described image determination data generation circuit.

Accordingly, the present application is deemed enabling. Reconsideration and withdrawal of the above rejection are respectfully requested.

Art-Based Rejections

In the Office Action, Claims 1-3, 7-9, 13-16, and 20-21 were rejected under 35 USC §102(b) over JP 408076721A (Kudo); Claims 1-3, 7-9, 13-16, and 20-21 were rejected under 35 USC §102(e) over US Patent Publication No. 2002/0018058 A1 (Tamura); Claims 5-6, 11-12, and 18-19 were rejected under 35 USC §103(a) over Kudo in view of US Patent No. 5,530,797 (Uya). Applicant respectfully traverses the above rejections and submits that the claims presented herein are patentable in light of the clarifying amendments above and the arguments below.

The Kudo Reference

Kudo is directed to a matrix display device which displays animation images and static images in combination. Kudo discloses a display driver comprised of a static picture display memory 104, a video data latch circuit 103, a data selector 105, a selection data latch circuit 106, and a liquid crystal drive circuit 107. *(See, Kudo; Figure 1).* The static picture display memory 104 stores the static picture data 116 and outputs the still picture data for 1 scan electrode to the data selector 105. *(See, Kudo; Paragraph [0017]).* The video latch circuit 103 sequentially

latches the video data 109 for a scan electrode and output the data to the data selector 105. The indicative-data 109a, which indicates the column positions of still picture, is incorporated as part of the video data 109. *(See, Kudo; Paragraph [0016]).* The data selector 105 selects between the still picture data and video picture for display base on the location data 109b of indicative-data 109a, both 109a and 109b being parts of video data 109. *(See, Kudo; Paragraph [0017]; Figure 6).*

The Tamura Reference

Tamura is directed to a RAM incorporated driver that enables the writing of the moving-image data and still-image data to the RAM simultaneously. Figure 12 of Tamura discloses a display driver comprised of a MPU-related control 130, a first display data RAM 310, a first column address control 142, a second display data RAM 320, a second column address control 144, and a selector 350. The first display data RAM 310 stores still-image data in column locations determined by the first column address control 142. The second display data RAM 320 stores moving-image data in column locations determined by the second column address control *(See, Tamura; Figure 5; Paragraph [0152]).* The outputs of the first display data RAM 310 and the second display data RAM 320 are selected by the selector 350 with controls generated by MPU-related control 130. Tamura does not teach the method of generating the controls of the selector 350.

The Uya Reference

Uya is directed to a workstation for video display to display simultaneously a plurality of video dynamic images. Uya discloses a system comprised of a static-image memory 1, a dynamic-image memory 2, a key plane memory 34, and a selector 6 *(See, Uya; Figure 8; Col. 1, lines 49-54).* The selector 6 selects between the static-image memory 1 and the dynamic-image memory 2 for display base on the key data in the key plane memory 34. *(See, Uya; Col. 2, lines 3-11).*

The Claims are Patentable Over the Cited References

The present invention is generally directed to a display driver that enables the simultaneous display of a still image and a moving image on the same scan line.

As defined by independent Claim 1, a display driver which drives a display section based on still-image data and moving-image data includes a random access memory (RAM) from which still-image data is read out for each scan line. A line memory stores moving-image data in scan line units. A selector selects and outputs one of a scan line output from the RAM and a line memory output for each column position based on image determination data. A line data register stores line data indicating whether or not the display section is to be driven based on the moving-image data at each scan line of one column. A column data register stores column data indicating whether or not the display section is to be driven based on the moving-image data at each column position of one scan line. A data generation circuit generates the image determination data based on the line data and the column data for each column position of one scan line in the display section. The image determination data is generated according to a column position defining a display area that is driven on the basis of the moving-image data or the still-image data, for each scan line.

The applied references do not disclose or suggest the above features of the present invention as defined by amended independent Claim 1. In particular, the applied references do not disclose or suggest, "a line data register which stores line data indicating whether or not the display section is to be driven based on the moving-image data, at each scan line of one column," as required by amended independent Claim 1.

Moreover, the applied references do not disclose or suggest, "a column data register which stores column data indicating whether or not the display section is to

be driven based on the moving-image data, at each column position of one scan line," as required by amended independent Claim 1.

Furthermore, the applied references do not disclose or suggest, "a data generation circuit which generates the image determination data based on the line data and the column data, for each column position of one scan line in the display section," as required by amended independent Claim 1.

Moreover, the applied references do not disclose or suggest, "wherein the image determination data is generated according to a column position defining a display area that is driven on the basis of the moving-image data or the still-image data, for each scan line," as required by amended independent Claim 1.

The applied Kudo reference discloses a video data latch circuit 103 that serially latches the moving-image data. The video data latch circuit 103 outputs a line of the moving-image data to the data selector 105. According to Kudo, the image determination data and the moving-image data are combined into a single bus 109, which is latched by a single input buffer 103 and controlled by a single clock 120. *(See, Kudo; Figure 1; Paragraph [0016]).* Kudo does not teach a memory between the video data latch circuit 103 and the data selector 105. *(See, Kudo, Figure 1).* Kudo fails to teach or suggest a line memory in the display driver as required by present application.

Moreover, according to Kudo, the video latch circuit 103 sequentially latches the video data 109 for a scan electrode and output the data to the data selector 105. The indicative-data 109a, which indicates the column positions of still picture, is incorporated as part of the video data 109. *(See, Kudo; Paragraph [0016]).* The data selector 105 selects between the still picture data and video picture for display base on the location data 109b of indicative-data 109a, both 109a and 109b being parts of video data 109. *(See, Kudo; Paragraph [0017]; Figure 6).*

In contrast, the present invention discloses a shift register 62 to serially latch the moving-image data. The shift register 62 outputs a line of the moving-image data to the line memory 26. The line memory 26 outputs a line of moving-image data to the selector 64. *(See, Specification; Figure 3).* Separate buses are used for the image determination data and the moving-image data. *(See, Specification; Figure 3).* The present invention further discloses a display driver having a display data RAM 24, a shift register 62, a line memory 26, and a selector 64, as shown in Figure 3 of the present application. The display data RAM stores the still-image data, and the shift register 62 is the serial input buffer of moving-image data. The line memory 26 stores the moving-image data in unit of lines, and the selector 64 selects between the outputs of the display data RAM 24 and the line memory 26 for display base on the image determination data. The image determination data and the moving-image data are on separate buses. *(See, Specification; Figure 3; Page 16-18).* The present invention further includes a driver-system control 170, which contains the image determination data generation circuit, as shown in Figure 9 of the present application. *(See, Specification; Page 28, lines 12-14).* Moreover, Figure 10 of the present application shows an image determination data RAM 220. These features of the present invention are not disclosed or suggested by Kudo.

Moreover, the present invention discloses that the display driver includes a line data register and a column data register, and one of moving-image data and still-image data is selected and output based on line data and column data. Kudo does not teach or suggest the line data and column data of the present invention. Kudo does not teach nor suggest the line data register, which stores line data, and the column data register, which stores column data, as recited in the claims of the present invention. The present invention enables the generation of image determination data using line data of bits corresponding to the number of columns and column data of bits corresponding to the number of lines. In this way, the

present invention can reduce the size of the circuit which stores line data and column data. As a result, the present invention can display moving and still images on the same scan line without complicating the circuit structure and with a low power consumption. *(See, Specification; Page 24, lines 9-16).* Kudo does not disclose or suggest the above features of the present invention as recited in the claims.

The ancillary Uya reference does not remedy the deficiencies of Kudo. In particular, Uya does not teach or suggest a line memory between the input buffer and the selector. Accordingly, the combination of Kudo and Uya fails to teach or suggest the subject matter of the claims of the present invention.

Similarly, the Tamura reference does not disclose or suggest the above features of the present invention. Tamura is directed to a RAM incorporated driver that enables the writing of the moving-image data and still-image data to the RAM simultaneously. Figure 12 of Tamura discloses a display driver comprised of a MPU-related control 130, a first display data RAM 310, a first column address control 142, a second display data RAM 320, a second column address control 144, and a selector 350. The first display data RAM 310 stores still-image data in column locations determined by the first column address control 142. The second display data RAM 320 stores moving-image data in column locations determined by the second column address control. *(See, Tamura; Figure 5; Paragraph [0152]).* The outputs of the first display data RAM 310 and the second display data RAM 320 are selected by the selector 350 with controls generated by MPU-related control 130. Tamura discloses a second display data RAM 310 of a fixed size for storing one frame of moving-image data *(See, Tamura; Paragraph [0148]).* Data is written into the second display data RAM 310 in column locations decoded by a second column address control 144. *(See, Tamura; Paragraph [0152).* Tamura fails to teach or suggest, "a line memory in which is stored moving-image data in scan line units," as required by amended independent Claim 1 of present invention.

In contrast, the present invention discloses a line memory 26 of unrestricted number of lines for storing moving-image data. Data is written in the line memory 26 in unit of a line. *(See, Specification; Figure 3).* Tamura does not disclose or suggest the above features of the present invention as recited in the claims.

Since the applied references do not disclose, teach, or suggest the above features as required by amended independent Claim 1, those references cannot be said to anticipate nor render obvious the invention which is the subject matter of amended independent Claim 1.

Accordingly, independent Claim 1, as amended, is believed to be in condition for allowance and such allowance is respectfully requested.

The remaining Claims 2, 5-8, 11-15, and 18-20 depend either directly or indirectly from amended independent Claim 1 and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references. Thus, the remaining Claims 2, 5-8, 11-15, and 18-20 are also believed to be in condition for allowance and such allowance is respectfully requested.

Conclusion

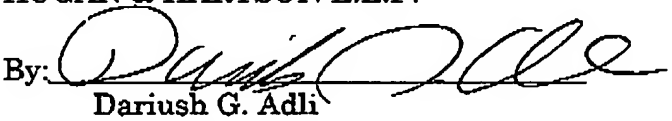
In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: November 8, 2004

By: 
Dariush G. Adli
Registration No. 51,386
Attorney for Applicant(s)

500 South Grand Avenue, Suite 1900
Los Angeles, California 90071
Phone: 213-337-6700
Fax: 213-337-6701